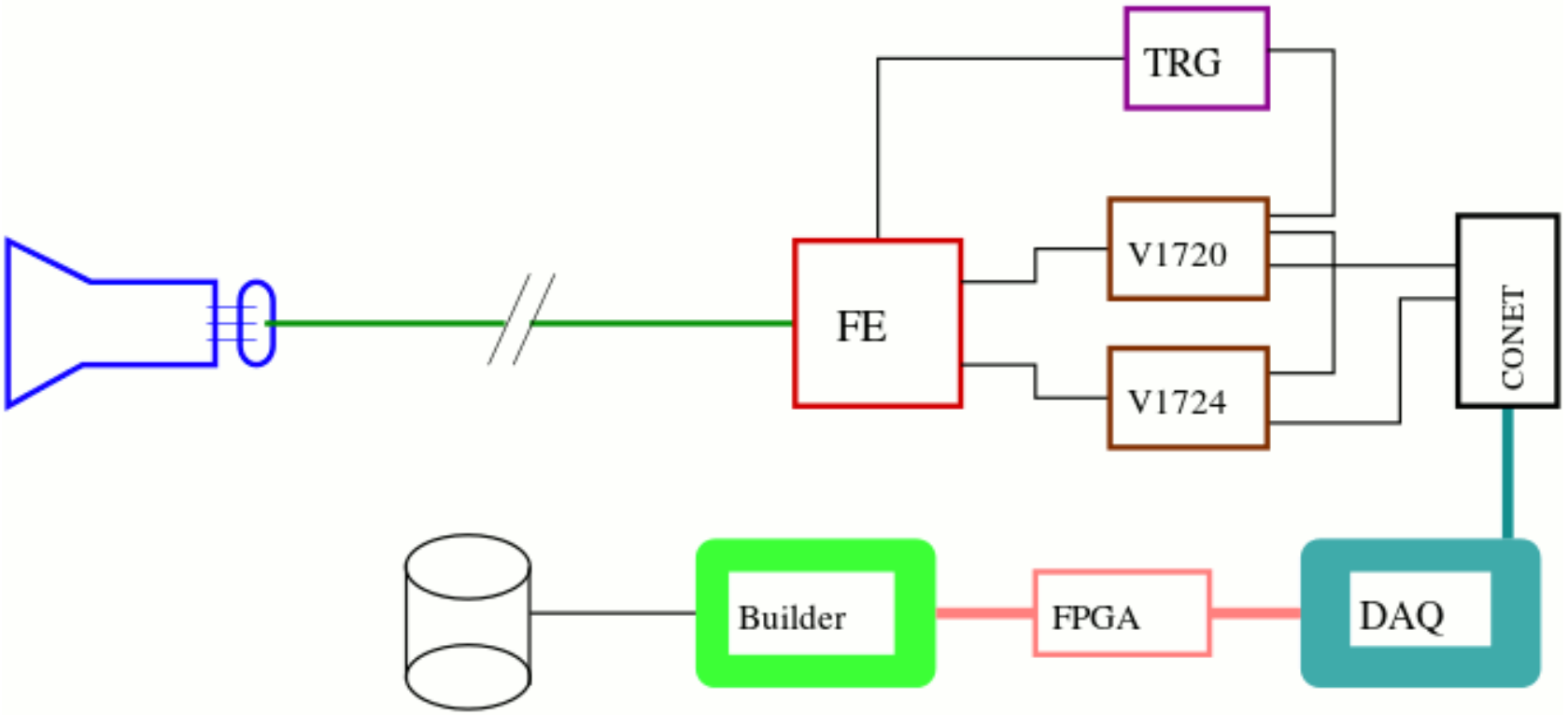
DS50 TPC readout

General structure



Proposal

- The presentation covers the current status of the design
- The design is not frozen but we have to start soon the implementation (deadline end 2012)
- The design is split in different parts
  - PMT + base
  - TPC cables
  - Front-end & shaper
  - Trigger unit
  - Digitizers + PCIe bridge
  - DAQ
  - Data reduction
  - Event Building
  - Storage

PMT & base

People

Pordes & others @FNAL, M. Orsini, Y. Suvorov, M. D'Incecco, G. Korga

- PMT & base already defined
  - Base developed at FNAL.
- In the next weeks @ LNGS we will:
  - Acquire single p.e. pulse shape
  - Acquire single p.e. charge shape
  - Test cold amplifier (R&D)
    - With different coupling than 50 Ohm
- These tests are different from the Napoli setup
  - We will use very short cables (RG2230)
  - A fast amplifier
  - A low noise 2 GHz oscilloscope
- What we want to obtain:
  - Single p.e. signal shape & power spectrum, signal amplitude, PMT charge resolution in the BEST condition
  - Electronic model for the PMT for simulation and for cold amplifier development

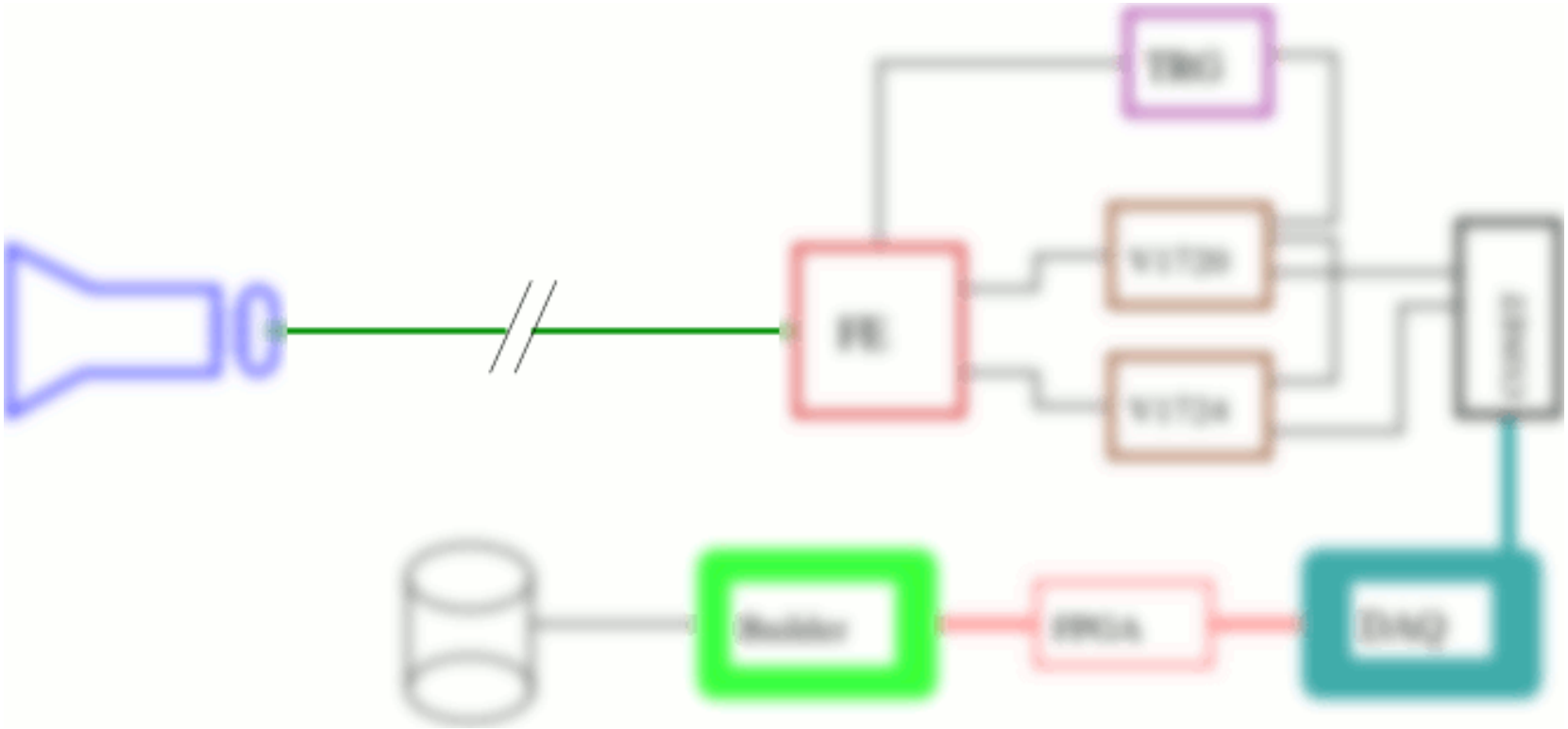
PMT Base

- What is the status?
  - We would like to test the PMT parameters with the final configuration
    - When the base will be ready?
- Initial studies done at al LNGS (G. Bonfini, A. Candela, D. Sabblone)
- Component for PMT base already screened
- We will screen other components:
  - We have tested very good capacitors FILM and COG capacitors
  - We are buying metal thin film resistors from Susumu
    - Thin film have very low temperature coefficient
    - In principle should be radiopure
- Suggestion: do not use resistor smaller than 0805, they could break in cold
- Did mass production already started?
  - We could foresee a small pod to plug the cold amplifier (if it will be needed)

Cold Amplifier R&D

- The project is to develop a preamplifier
  - High radiopure ← simple design very few components
  - Gain 10x with custom input impedance matching
  - Working in LN2 with a power dissipation < 0.5 Watt
- The project started for QUPIDs but now it moved to PMTs
- It is not intended for DS50 but
  - It is now very hard to predict the electronic noise in DS50, while the SPE is ~ 2mV
  - We want to continue the development as an alternative
- R&D status:
  - Funding from INFN GR5
  - Amplifier working in LN2 (very low noise) and @ room temperature
  - Dynamics up to 200 mV input
  - Check in Naples facility in July
  - Check for impedance matching with PMT in next weeks
  - Radiopurity tests starting soon

TPC cables



People

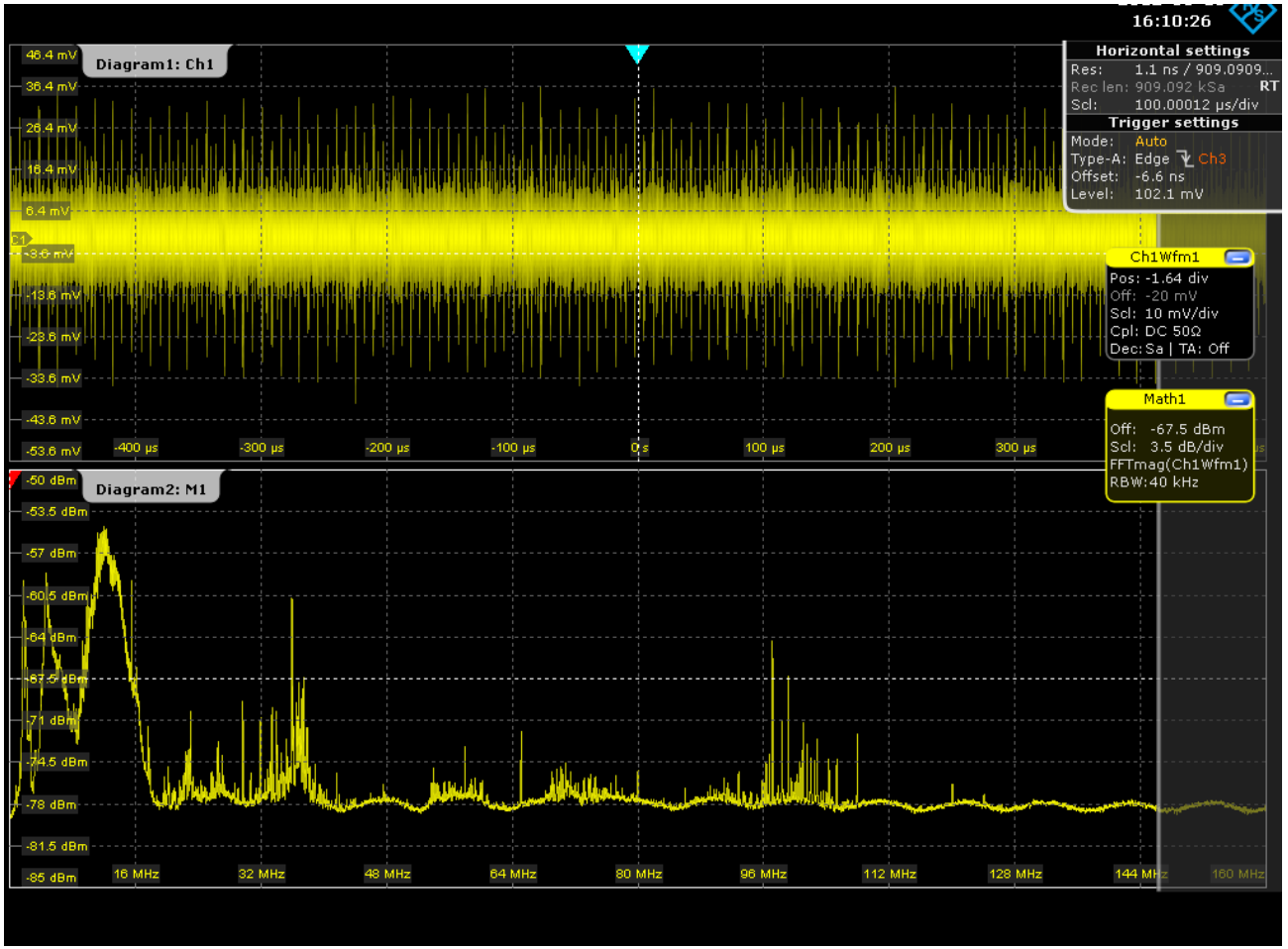
A. Candela, G. Bonfini, J. Martoff, M. Laubenstein

- TPC cables not yet defined
- TPC cables parameters:
  - Working in LAr
  - High radiopurity
  - Compatible with AccuGlass connectors
  - Low loss
  - Double shielding
- In LNGS we are starting a screening of the following cables (all teflon based):
  - RG316 Shuner (normal and double shielded)
  - SFT316
  - Multiflex 86
- We will check:
  - Radiopurity (Mathias already in touch)
  - PMT signal attenuation & noise shielding (with a real PMT)
  - Tests in LN2

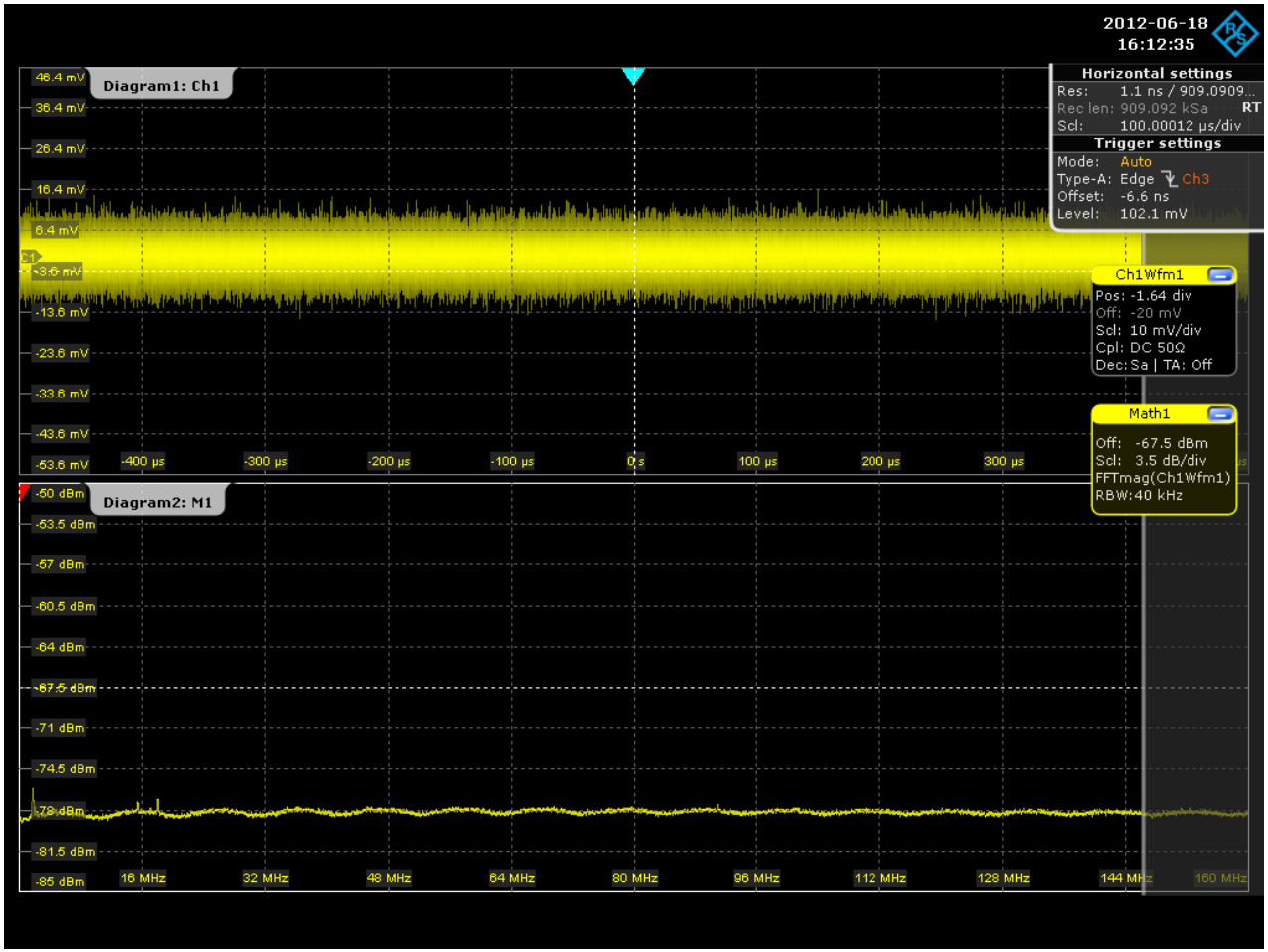
Double shielding

- PMT signal is ~ 2 mV
- Noise on a RG174 can contribute up to 0.5 mV RMS
  - We see this in DS10 where the SER contains a noise contribution
- CTF tank is a shielding but we inject noise
  - All unshielded cables entering
  - Ground loop
  - HHV noise
- In our test we will report the noise entering 10m of the 4 cables under test
- AccuGlass: Pino and Jeff are already in touch with Accuglass to verify the feasibility of double shielded cables
  - The first feedback is positive

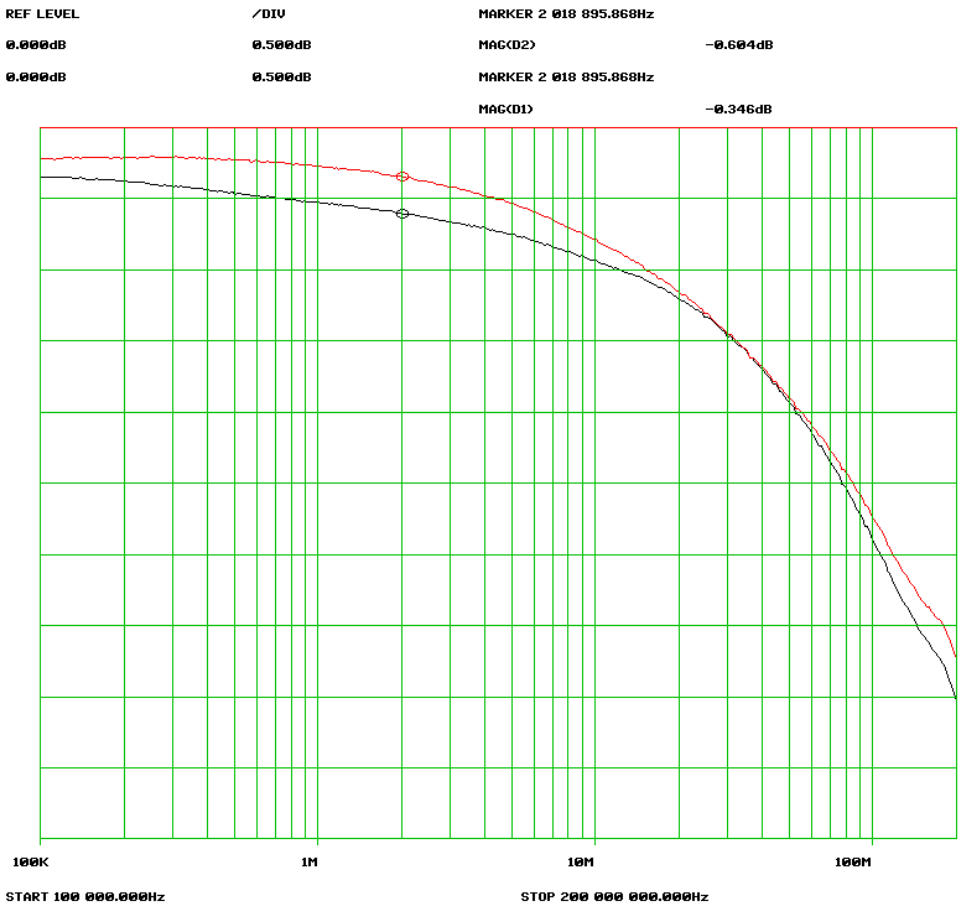
Single shielded RG316



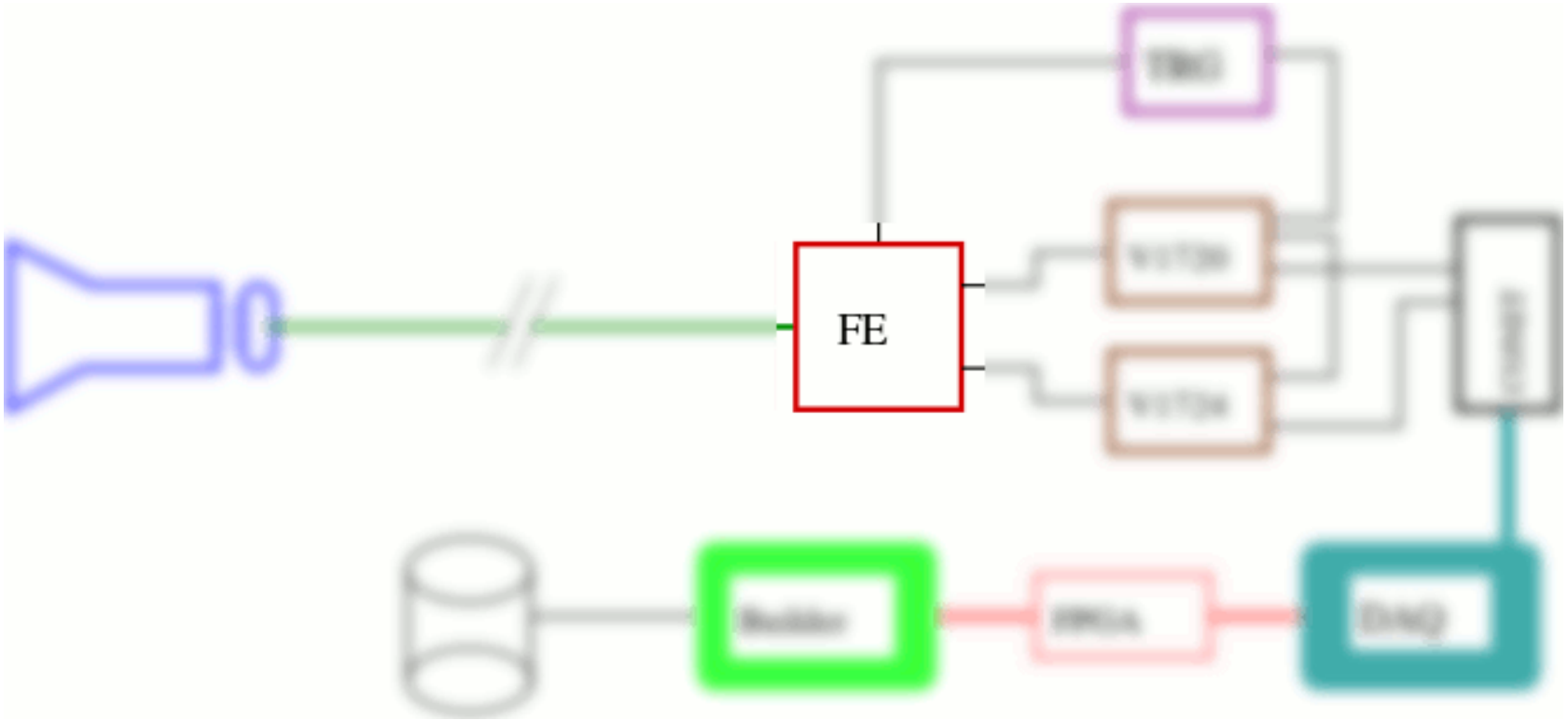
Double shielded RG316



RG316 & Multiflex 86



Front-End and shaper



People

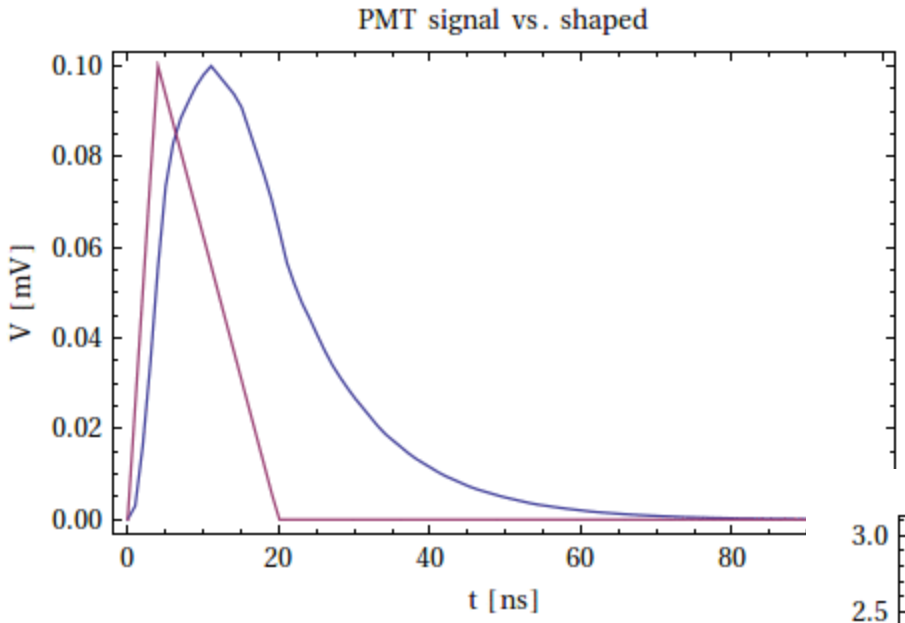
M. D'Incecco, G. Korga, A. Razeto

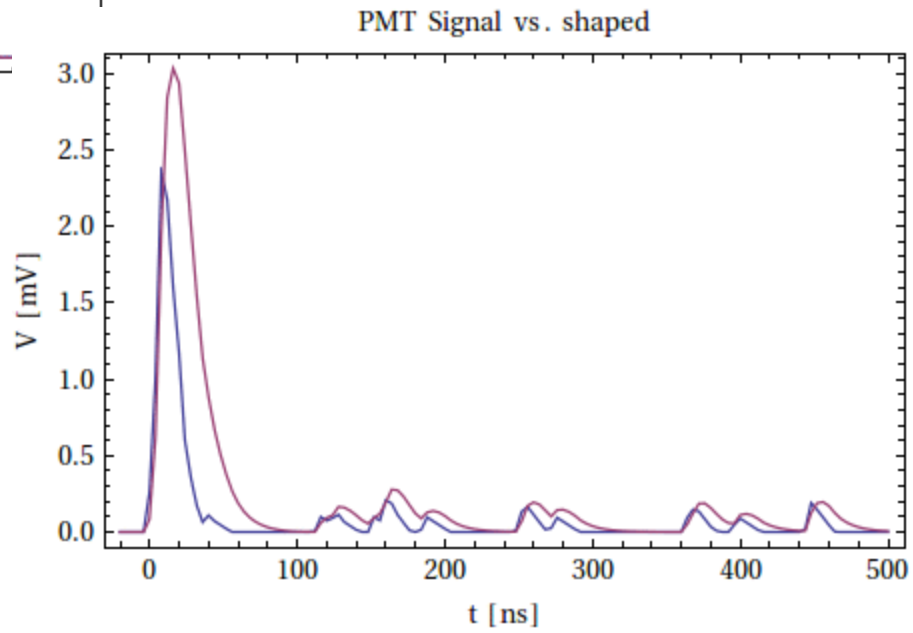
- We will start from the Genova boards which have:
  - LVDS discriminators (to trigger unit)
  - Scalers to monitor each channel
  - Software (from Genova)
  - A housing mechanics + power supply
- We will redesign the input stage:
  - To directly produce the shaped signals
- Some simulations already started
- In next week we will have some preliminary shaping amplifier
- When all the parameters will be fixed we will do a first run of PCB with only the analog stage
  - We will test the performance of the shaping amplifier within DS10
- When the design will be finalized we will put the PCB in the Genova boards for the board production

Shaping amplifier

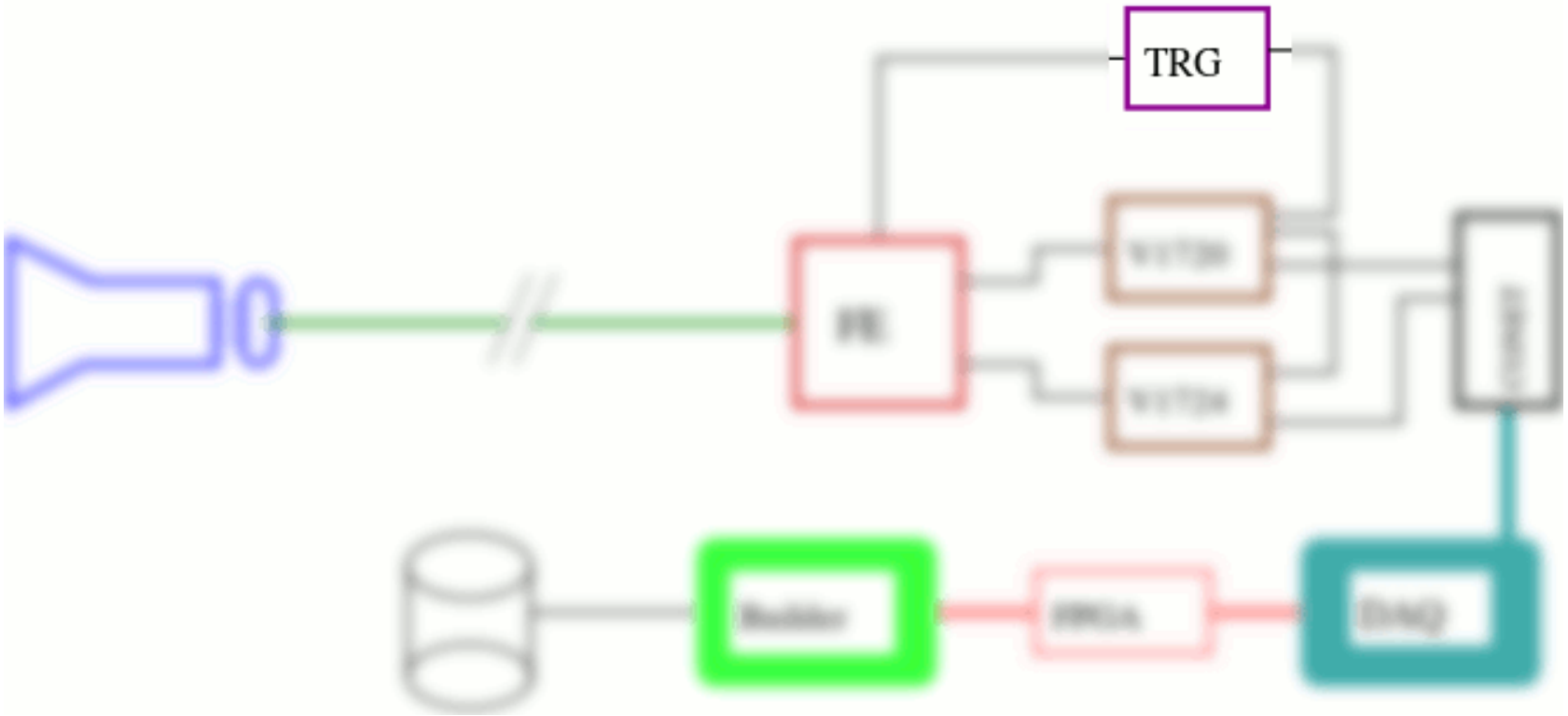
- The proposed shaper is a bandwidth limited amplifier
- 2 different circuit:
  - Amplified signal: gain x8, cut at ~30MHz
  - Attenuated signal: gain %5, cut at ~15MHz
- With these parameters the readout will be capable to acquire 2.6 MeV electron recoil and 8 MeV alphas (see technical document)
- The goal for the amplifier noise is to have better than 10 % resolution on spe like signal.

Example of shaped signal





Trigger Unit



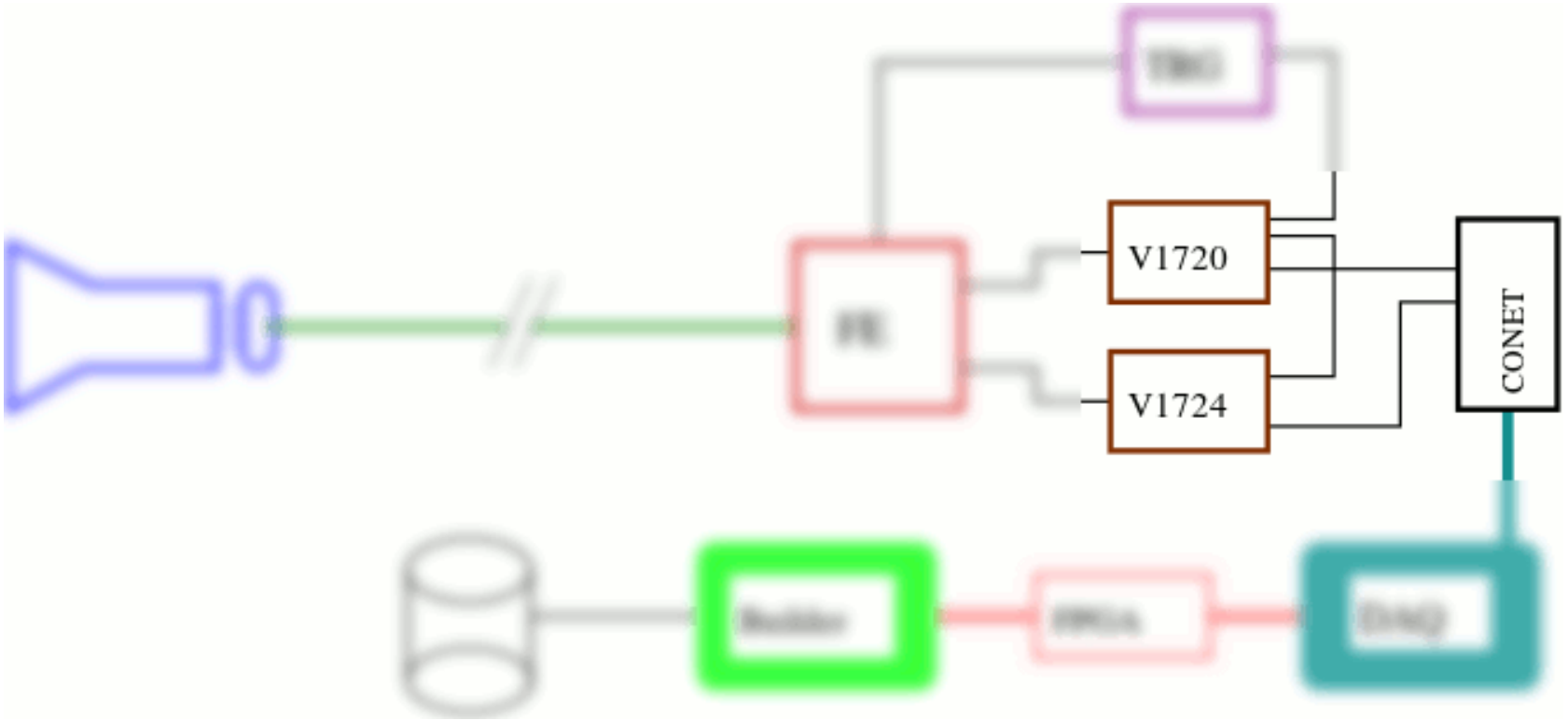
People

G. Bonfini, M. De Deo, JinYuan Wu

- The trigger unit (TU) will be based on V1495
- The TU will provide
  - Trigger signal
  - Run logic
  - Event number
  - Signal to/from vetoes
- The module will use as input the discriminator signal
- Smart trigger algorithms will be developed
  - Trigger only on S1
  - Trigger only on S2
  - Trigger on S2/S1
- It is indeed possible in the TU to evaluate the charge for both S1 and S2
- It will be possible to decimate high energy events

We need a licence for Altera Quartus

Digitizers



People

P. Cavalcante, M. De Deo, P. Saggese, A Razeto

- Digitizers already defined:
  - V1720 for amplified signal: 250 MS/s 12 bit
  - V1724 for attenuated signal: 100 MS/s 14 bit
    - **Not a problem for S2 (slow signal)**
    - **For S1 we will shape a bit more**
- We prefer not to touch the FPGA on the digitizers
  - Data reduction will be done later (by devoted code/ HW)
- We have to measure noise parameters of the boards:
  - ENOB, noise spectral power
- Tests starting on next weeks:
  - CONET protocol verification
    - Leaving a small proto-DAQ running at full speed for 2 weeks
  - CAEN digitizer lib
    - Is it working?

Workbench

- We have to setup as soon as possible a setup for the tests
- Some of the hardware will be the final one
  - The DAQ computers in particular
    - 3 machine for the DAQ (1 every 4 digitizers i.e. 1 every CONET2 board)
    - 1 machine for building
    - P. Saggese already asking for quotes
  - Some of the hardware is arriving (V1720)
- We have to buy soon some equipment (or to loan it)
- The workbench will provide the full readout chain from PMT to disk
  - P. Cavalcante in charge

DAQ

People

P. Cavalcante, A Razeto

Bandwidths

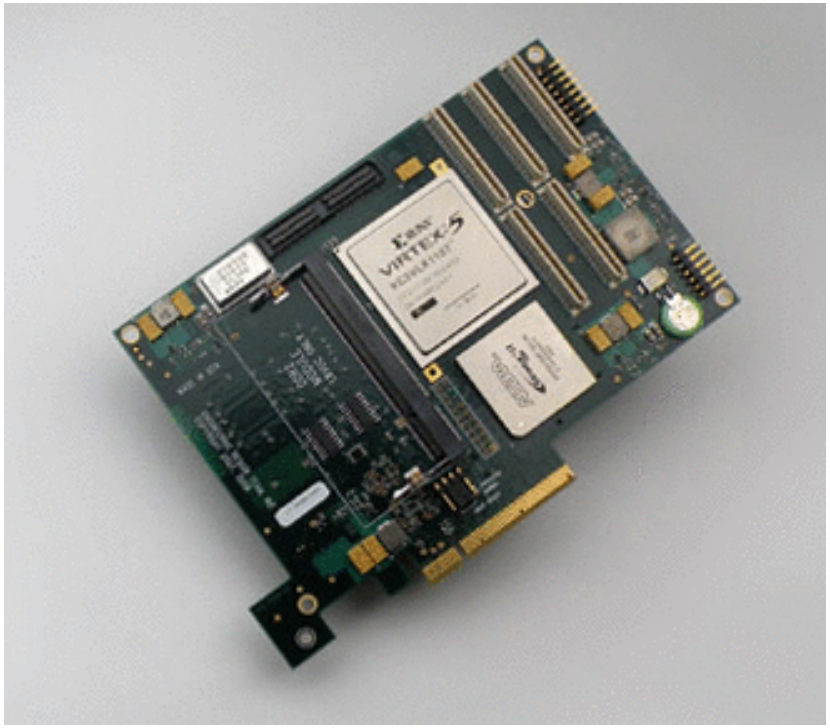
- We have:
  - 38 x 2 channels (250/100 MS/s)
  - Acquisition gate **300 μs** -> **8MB/event**
  - Normal operation (10 Hz)
    - In a day 7 TB/day data
    - In a second 640 Mb/s
      - LNGS connection is/will be 1Gb/s for all experiments
    - Per board 100 Mb/s/board (CONET is 1 Gb/s)
  - Calibration 100 Hz -> ? What ? Are u kidding ?
- Disk:
  - At 10 Hz
    - 3TB disk last 10 hour
    - 1 disk = 500 $ (including a storage unit)
  - 1 year of data = 500 000 $ in disks
  - 10 calibration days = 120 000 $ in disks
- CPU:
  - To analyze all that we need probably ~ 500 000 $ cluster

Data reduction

- My proposal is the following:
  - S1 will be kept as it is for 3 us
    - 80 kB/event
  - S2 will be down sampled at 10 MHz
    - After digital filter at 0.2 MHz (i.e. 600 ns cut)
    - 80 kB/event for 100 us S2
  - Baseline will be zero suppressed
    - After subtracting the floating baseline
    - 10 kB/event (depending on the noise)
  - Total digital sum for upper and lower PMTs
    - 400 kB/event
  - In total ~ 600 kB/event
- Adding data compression of factor 5
  - 100 kB/event -> 90 GB/day (~ 10 Mb/s on network)

- The total CPU power for this operation can be very high
  - It is not clear if the DAQ computer can cope
- Data reduction will be done on a PCIe FPGA
  - FPGA can easily perform all the tasks fast
- A library shall be implemented to communicate with the FPGA

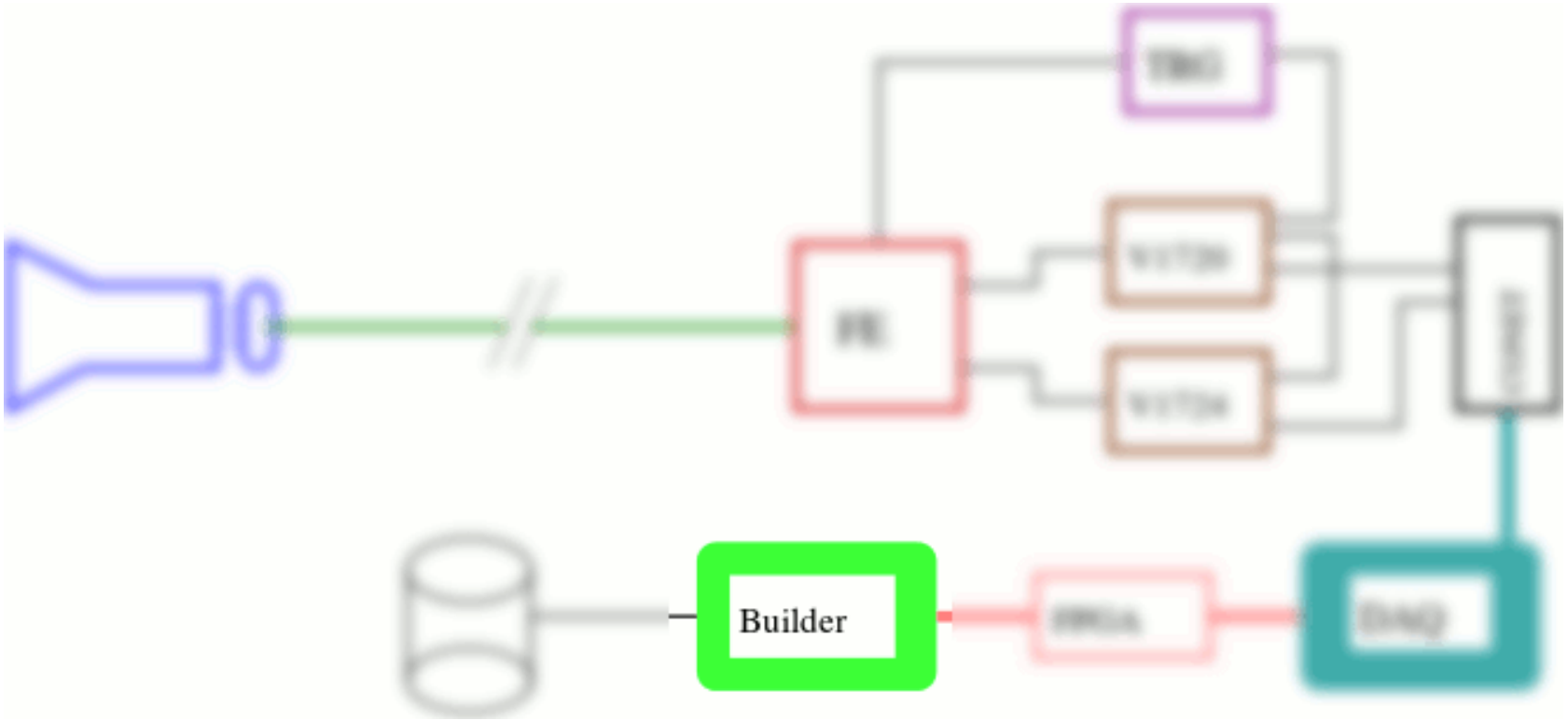
- As alternative this can be implemented in SW within ARTDAQ
- Who can take care of it?



DAQ software

- New very slim code
- In C++11
- Doing parallel I/O

Builder



People
FNAL ???

- It could/should be a very simple code
  - No veto integration
  - Events are already tagged with an unique id (from TU)
- Or we use artdaq:
  - **In this case FNAL will be in charge to implement, debug and to maintain it**

- Data compression is a must in any case

Rack & mounting

- The positioning of all the electronics devices has to be carefully studied
  - Front-End and Digitizers will be installed in the clean room
  - The acquisition computers can be hosted in the same rack
- We need a detailed schematics of what we have to install and where

- A. Candela could be the man

Needed

- Software:
  - Microcap floating license
    - For electronics simulation
  - Matlab floating license
    - For filter check and other simulations
  - Altera Quartus
    - For trigger unit
- HW:
  - 1 development VME crate
  - 1 PMT
  - Arbitrary function generator
- DAQ:
  - 3 rack computers for DAQ (buy soon)
  - 5-7 rack computers for building/zero suppressio/compression (from FNAL specs)
  - 2x 10 GB switch + double optical connection

Man Power

- Simulation:
  - N. Rossi, Suerfu
- Cables + Rack:
  - A. Candela, G. Bonfini
- Shaper and FrontEnd
  - M. D'Incecco, G. Korga
- Trigger
  - G. Bonfini, M. De Deo, Jinyuan Wu
- DAQ
  - P. Cavalcante, A. Razeto
- Data Reduction and builder
  - FNAL (1 FTE) + A. Razeto